WEST Search History

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DATE: Wednesday, November 19, 2003

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT,PGPB,JPAB,EPAB,DWPI,TDBD; PLUR=YES; OP=ADJ		
L11	('US 5307351A')[ABPN1,NRPN,PN,TBAN,WKU]	1	L11
L10	('JP02001244947A')[ABPN1,NRPN,PN,TBAN,WKU]	1	L10
L9	('5307351')[ABPN1,NRPN,PN,TBAN,WKU]	2	L9
L8	$3assembl$3 with (sub$1block or super$1block or sub$1packet or super$1packet or super$1fram$4 or sub$1fram$4 or block or packet or fram$4 or divi$6 or re$1partition$4 or partition$4 or break$4 or segment$7 or fragment$6) same (program$7 or adjust$6 or vari$4 or vary$4 or configur$7 or re$1configur$7 or re$1defin$6 or chang$7 OR ALTER$7) near2 (length or wid$3 or size) same (error or fail$3 or noisy) near2 (rate or ratio)	4	L8
L7	('20030188249')[ABPN1,NRPN,PN,TBAN,WKU]	2	L7
L6	L5 not l4	1	L6
L5	L2 and (iterat$7 or recur$7 or serial or parallel or convolution$4 or concatenat$4 or turbo or pccc) near2(cod$3 or encod$3 or decod$3) same (sub$1block or super$1block or sub$1packet or super$1packet or super$1fram$4 or sub$1fram$4 or block or packet or fram$4 or divi$6 or re$1partition$4 or partition$4 or break$4 or segment$7 or fragment$6) same (program$7 or adjust$6 or vari$4 or vary$4 or configur$7 or re$1configur$7 or re$1defin$6 or chang$7 OR ALTER$7) near2 (length or wid$3 or size) same (error or fail$3 or noisy) near2 (rate or ratio)	3	L5
L4	('6166667'| '4201958')[ABPN1,NRPN,PN,TBAN,WKU]	5	L4
L3	L2 and (iterat$7 or recur$7 or serial or parallel or convolution$4 or concatenat$4 or turbo or pccc) near2(cod$3 or encod$3 or decod$3) same (sub$1block or super$1block or sub$1packet or super$1packet or super$1fram$4 or sub$1fram$4 or block or packet or fram$4 or divi$6 or re$1partition$4 or partition$4 or break$4 or segment$7 or fragment$6) same variable near2 (length or wid$3 or size) same (error or fail$3 or noisy) near2 (rate or ratio)	2	L3
L2	L1 and (iterat$7 or recur$7 or serial or parallel or convolution$4 or concatenat$4 or turbo or pccc) near2(cod$3 or encod$3 or decod$3) same (sub$1block or super$1block or sub$1packet or super$1packet or super$1fram$4 or sub$1fram$4 or block or packet or fram$4 or divi$6 or re$1partition$4 or partition$4 or break$4 or segment$7 or fragment$6) same variable near2 (length or wid$3 or size)	262	L2
L1	(iterat$7 or recur$7 or serial or parallel or convolution$4 or concatenat$4 or turbo or pccc) near2(cod$3 or encod$3 or decod$3) same (sub$1block or super$1block or sub$1packet or super$1packet or super$1fram$4 or sub$1fram$4 or block or packet or fram$4 or divi$6 or re$1partition$4 or	10642	L1

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partition$4 or break$4 or segment$7 or fragment$6)

END OF SEARCH HISTORY

L8: Entry 20 of 30 File: USPT Feb 10, 1998

DOCUMENT-IDENTIFIER: US 5717394 A
TITLE: Method and apparatus for encoding and decoding data

Detailed Description Text (32):
The solution offered in this invention separates the problem of distributing the coded data to the parallel coders from the alignment of the variable-length codewords for decoding. The codewords in each independent code stream are packed into fixed-length words, called interleaved words. At the decoder end of the channel these interleaved words can be distributed to the parallel decoder units with fast hardwired data lines and a simple control circuit.

Detailed Description Text (194):
The input variable length data is divided into fixed length interleaved words such as described in conjunction with FIG. 4. The decoder uses the fixed length words as described in FIG. 16A below. The decoder and delay models a pipeline decoder as described in conjunction with FIGS. 15 and 32 or multiple parallel decoders such as described in conjunction with FIGS. 2A-2D. Thus, the present invention provides a delay tolerant decoder. The delay tolerant decoders of the present invention allow handling of variable length data in parallel.

L3: Entry 9 of 10 File: USPT Mar 26, 1996

DOCUMENT-IDENTIFIER: US 5502736 A
TITLE: Viterbi decoder for decoding error-correcting encoded information symbol string

Abstract Text (1):
A Viterbi decoder includes a first inverse mapping circuit, first to fourth branch metric generators, first to eighth accumulator switch circuits (ACS circuits) with one ACS circuit corresponding to one of the eight states of the feedback-type convolutional encoder, a path memory, and a re-encoder for the purpose of decoding an influential bit and a redundant bit of 4-bit error-correcting encoded information symbol string from I-channel data and Q-channel data. A Viterbi decoder also includes first and second shift registers having a number of levels determined according to the delay in the re-encoder and the delay in the path memory and a second inverse mapping circuit for the purpose of decoding noncoding bits of 4-bit error-correcting encoded information symbol string using the I-channel data and the Q-channel data.

Brief Summary Text (8):
A Viterbi decoder 30 shown in FIG. 1 includes an inverse mapping circuit 33, first to fourth branch metric generators 34.sub.1 -34.sub.4, first to eighth accumulator switch circuits (hereinafter referred to as ACS circuits 35.sub.1 -35.sub.8), of which one circuit corresponds to one of the eight states of the feedback-type convolutional encoder, a path memory 36, a re-encoder 37, first to fourth shift registers 38.sub.1 -38.sub.4 having a number of levels set with consideration taken for the delay in the re-encoder 37 and the delay in the path memory 36, and a selector 39. The transmitted signal sent from a transmitter to a receiver is converted to two demodulated signals by means of orthogonal synchronous detection carried out by a orthogonal synchronous detector (not shown) of the receiver. Each of the two demodulated signals is converted to m-bit I-channel data Ich and m-bit Q-channel data Qch by the quantization of their amplitude values by a quantizing circuit (not shown). Here, I-channel data Ich and Q-channel data Qch are 2m-value soft decision data. I-channel data Ich and Q-channel data Qch are both inputted to the inverse mapping circuit 33 by way of two input terminals 31, 32. In the inverse mapping circuit 33, the representative symbol points of subsets A, B, C, and D are found from I-channel data Ich and Q-channel data Qch. Each of the found representative symbol points of subsets A, B, C, and D is inverse mapped onto 4-bit data corresponding to it. The noncoding bits which are the two higher-order bits of the 4-bit data inverse mapped for subset A are inputted to the first shift register 38.sub.1. The noncoding bits which are the two higher-order bits of the 4-bit data inverse mapped for subset B are inputted to the second shift register 38.sub.2. The noncoding bits which are the two higher-order bits of the 4-bit data inverse mapped for subset C are inputted to the third shift register 38.sub.3. The noncoding bits which are the two higher-order bits of the 4-bit data inverse mapped for subset D are inputted to the fourth shift register 38.sub.4.

Detailed Description Text (2):
As shown in FIG. 2, a Viterbi decoder 20 according to an embodiment of the present invention comprises a first inverse mapping circuit 3, first to fourth branch metric generators 4.sub.1 -4.sub.4, first to eighth accumulator switch circuits (hereinafter referred to as ACS circuits 5.sub.1 -5.sub.8) with one ACS circuit corresponding to one of the eight states of the feedback-type convolutional encoder, a path memory 6, a re-encoder 7, first and second shift registers 8.sub.1, 8.sub.2 having a number of levels determined according to the delay in the re-encoder 7 and the delay in the path memory 6, and a second inverse mapping circuit 10.